IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE

IEEE

Membership Publications/Services Standards Conferences Careers/Jobs

IEEE Xplore® RELEASE 1.8

Welcome
United States Patent and Trademark Office

» Se

Help FAQ Terms IEEE Peer Review Quick Links

Welcome to IEEE Xplore

- Home
- What Can I Access?
- Log-out

Tables of Contents

- Journals & Magazines
- Conference Proceedings
- Standards

Search

- By Author
- Basic
- Advanced

Member Services

- Join IEEE
- Establish IEEE Web Account
- Access the IEEE Member Digital Library

IEEE Enterprise

- Access the IEEE Enterprise File Cabinet

Print Format

Your search matched **42** of **1075719** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enter new one in the text box.

test <and> pattern <and> automatic <and> output <and> Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

1 **Masking of unknown output values during output response compre by using comparison units**
Pomeranz, I.; Sandip Kundu; Reddy, S.M.;
Computers, IEEE Transactions on , Volume: 53 , Issue: 1 , Jan 2004
Pages:83 - 89

[Abstract] [PDF Full-Text (362 KB)] IEEE JNL

---

2 **Test data compression based on input-output dependence**
Pomeranz, I.; Reddy, S.M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on , Volume: 22 , Issue: 10 , Oct. 2003
Pages:1450 - 1455

[Abstract] [PDF Full-Text (476 KB)] IEEE JNL

---

3 **Synthesis of single-output space compactors for scan-based seque circuits**
Bhattacharya, B.B.; Dmitriev, A.; Gossel, M.; Chakrabarty, K.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on , Volume: 21 , Issue: 10 , Oct. 2002
Pages:1171 - 1179

[Abstract] [PDF Full-Text (322 KB)] IEEE JNL

---

4 **Automated synthesis of phase shifters for built-in self-test applicat**
Rajski, J.; Tamarapalli, N.; Tyszer, J.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on , Volume: 19 , Issue: 10 , Oct. 2000
Pages:1175 - 1188

[Abstract] [PDF Full-Text (320 KB)] IEEE JNL

5 **Space compaction under generalized mergeability**
Das, S.R.; Petriu, E.M.; Barakat, T.F.; Assaf, M.H.; Nayak, A.R.;
Instrumentation and Measurement, IEEE Transactions on , Volume: 47 , Issu
5 , Oct. 1998
Pages:1283 - 1293

[Abstract] [PDF Full-Text (580 KB)] IEEE JNL

6 **Automatic test pattern generation with branch testing**
Makki, R.Z.; Bou-Ghazale, S.; Tianshang, C.;
Computers, IEEE Transactions on , Volume: 40 , Issue: 6 , June 1991
Pages:785 - 791

[Abstract] [PDF Full-Text (504 KB)] IEEE JNL

7 **Digital components for built-in self-test of analog circuits**
Stroud, C.; Karunaratna, P.; Bradley, E.;
ASIC Conference and Exhibit, 1997. Proceedings., Tenth Annual IEEE
International , 7-10 Sept. 1997
Pages:47 - 51

[Abstract] [PDF Full-Text (544 KB)] IEEE CNF

8 **Testing iterative logic arrays for delay faults with a constant numb
patterns**
Shyue-Kung Lu; Mau-Jung Lu;
Electronic Materials and Packaging, 2002. Proceedings of the 4th Internationa
Symposium on , 4-6 Dec. 2002
Pages:492 - 498

[Abstract] [PDF Full-Text (490 KB)] IEEE CNF

9 **Automatic test generation for analog circuits using compact test
transfer function models**
Sahu, B.; Chatterjee, A.;
Test Symposium, 2001. Proceedings. 10th Asian , 19-21 Nov. 2001
Pages:405 - 410

[Abstract] [PDF Full-Text (580 KB)] IEEE CNF

10 **Charge sharing fault detection for CMOS domino logic circuits**
Cheng, C.H.; Chang, S.C.; Wang, J.S.; Jone, W.B.;
Defect and Fault Tolerance in VLSI Systems, 1999. DFT '99. International
Symposium on , 1-3 Nov. 1999
Pages:77 - 85

[Abstract] [PDF Full-Text (160 KB)] IEEE CNF

11 **Feedback driven backtrace of analog signals and its application to
circuit verification and test**

Voorakaranam, R.; Chatterjee, A.;
Advanced Research in VLSI, 1999. Proceedings. 20th Anniversary Conference on , 21-24 March 1999
Pages:342 - 355

[Abstract] [PDF Full-Text (140 KB)] **IEEE CNF**

---

12 **A fault partitioning method in parallel test generation for large sca VLSI circuits**
Zhide Zeng; Jihua Chen; Pengxin Liu;
Test Symposium, 1999. (ATS '99) Proceedings. Eighth Asian , 16-18 Nov. 19
Pages:133 - 137

[Abstract] [PDF Full-Text (56 KB)] **IEEE CNF**

---

13 **A unified framework for generating all propagation functions for lo errors and events**
Michael, M.K.; Haniotakis, T.; Tragoudas, S.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on , Volume: 23 , Issue: 6 , June 2004
Pages:980 - 986

[Abstract] [PDF Full-Text (320 KB)] **IEEE JNL**

---

14 **Sequential fault modeling and test pattern generation for CMOS iterative logic arrays**
Psarakis, M.; Gizopoulos, D.; Paschalis, A.; Zorian, Y.;
Computers, IEEE Transactions on , Volume: 49 , Issue: 10 , Oct. 2000
Pages:1083 - 1099

[Abstract] [PDF Full-Text (512 KB)] **IEEE JNL**

---

15 **A system for recognizing a large class of engineering drawings**
Yuhong Yu; Samal, A.; Seth, S.C.;
Pattern Analysis and Machine Intelligence, IEEE Transactions on , Volume: 19 , Issue: 8 , Aug. 1997
Pages:868 - 890

[Abstract] [PDF Full-Text (592 KB)] **IEEE JNL**

---

1 2 3 Next

Copyright © 2004 IEEE — All rights reserved

	Document ID	Issue Date	Pages	Title	Current OR
1	US 20040193957 A1	20040930	69	Emulation devices, systems and methods utilizing state machines	714/30
2	US 20040177299 A1	20040909	22	Scalable scan-path test point insertion technique	714/726
3	US 20040128596 A1	20040701	16	Method and apparatus for testing embedded cores	714/724
4	US 20040073856 A1	20040415	13	Parametric testing for high pin count ASIC	714/727
5	US 20040073845 A1	20040415	14	Range based detection of memory access	714/42
6	US 20040064771 A1	20040401	19	Method and system for coding test pattern for scan design	714/733
7	US 20030196144 A1	20031016	74	Processor condition sensing circuits, systems and methods	714/34
8	US 20030188246 A1	20031002	12	Method and apparatus for deriving a bounded set of path delay test patterns covering all transition faults	714/738
9	US 20030182604 A1	20030925	20	Method for reducing switching activity during a scan operation with limited impact on the test coverage of an integrated circuit	714/715
10	US 20030131298 A1	20030710	19	Test pattern compression for an integrated circuit test environment	714/738
11	US 20020184560 A1	20021205	61	Multiple-capture DFT system for scan-based integrated circuits	714/25
12	US 20020073374 A1	20020613	31	Method,system and program product for testing and/or diagnosing circuits using embedded test controller access data	714/738
13	US 20020059541 A1	20020516	10	Automatic detection of connectivity between an emulator and a target device	714/28

	Document ID	Issue Date	Pages	Title	Current OR
14	US 20020053057 A1	20020502	19	Test pattern compression for an integrated circuit test environment	714/738
15	US 20020032898 A1	20020314	13	Computer implemented circuit synthesis system	716/18
16	US 20020013918 A1	20020131	68	Devices, systems and methods for mode driven stops	714/30
17	US 20010039633 A1	20011108	11	Dynamically configurable debug port for concurrent support of debug functions from multiple data processing cores	714/28
18	US 6782515 B2	20040824	16	Method for identifying test points to optimize the testing of integrated circuits using a genetic algorithm	716/4
19	US 6760866 B2	20040706	64	Process of operating a processor with domains and clocks	714/34
20	US 6754852 B2	20040622	17	Debug trigger builder	714/39
21	US 6738929 B2	20040518	11	Dynamically configurable debug port for concurrent support of debug functions from multiple data processing cores	714/28
22	US 6725391 B2	20040420	24	Clock modes for a debug port with on the fly clock switching	713/500
23	US 6704895 B1	20040309	64	Integrated circuit with emulation register in JTAG JAP	714/726
24	US 6671870 B2	20031230	13	Computer implemented circuit synthesis system	716/18
25	US 6662327 B1	20031209	30	Method for clustered test pattern generation	714/738

	Document ID	Issue Date	Pages	Title	Current OR
26	US 6631344 B1	20031007	15	Method and system for performing deterministic analysis and speculative analysis for more efficient automatic test pattern generation	703/22
27	US 6611933 B1	20030826	12	Real-time decoder for scan test patterns	714/726
28	US 6546505 B1	20030408	94	Processor condition sensing circuits, systems and methods	714/30
29	US 6543020 B2	20030401	20	Test pattern compression for an integrated circuit test environment	714/738
30	US 6539497 B2	20030325	65	IC with selectively applied functional and test clocks	714/30
31	US 6522985 B1	20030218	67	Emulation devices, systems and methods utilizing state machines	702/117
32	US 6385750 B1	20020507	13	Method and system for controlling test data volume in deterministic test pattern generation	714/738
33	US 6349392 B1	20020219	64	Devices, systems and methods for mode driven stops	714/30
34	US 6327687 B1	20011204	20	Test pattern compression for an integrated circuit test environment	714/738
35	US 6311318 B1	20011030	12	Design for test area optimization algorithm	716/18
36	US 6249893 B1	20010619	20	Method and structure for testing embedded cores based system-on-a-chip	714/741
37	US 6205407 B1	20010320	16	System and method for generating test program code simultaneously with data produced by ATPG or simulation pattern capture program	702/119
38	US 6085336 A	20000704	91	Data processing devices, systems and methods with mode driven stops	714/30
39	US 6041429 A	20000321	8	System for test data storage reduction	714/738

	Document ID	Issue Date	Pages	Title	Current OR
40	US 6032268 A	20000229	77	Processor condition sensing circuits, systems and methods	714/30
41	US 5991909 A	19991123	18	Parallel decompressor and related methods and apparatuses	714/729
42	US 5862149 A	19990119	23	Method of partitioning logic designs for automatic test pattern generation based on logical registers	714/726
43	US 5841670 A	19981124	87	Emulation devices, systems and methods with distributed control of clock domains	703/23
44	US 5805792 A	19980908	108	Emulation devices, systems, and methods	714/28
45	US 5802075 A	19980901	35	Distributed test pattern generation	714/738
46	US 5710934 A	19980120	32	Methods and test platforms for developing an application-specific integrated circuit	714/724
47	US 5684808 A	19971104	22	System and method for satisfying mutually exclusive gating requirements in automatic test pattern generation systems	714/726
48	US 5633812 A	19970527	20	Fault simulation of testing for board circuit failures	703/15
49	US 5539652 A	19960723	51	Method for manufacturing test simulation in electronic circuit design	703/14
50	US 5535331 A	19960709	107	Processor condition sensing circuits, systems and methods	714/45
51	US 5329471 A	19940712	83	Emulation devices, systems and methods utilizing state machines	703/23
52	US 4611320 A	19860909	48	Programmable testing analyzer	370/241
53	US 4519078 A	19850521	16	LSI self-test method	714/728
54	US 4348760 A	19820907	19	Digital-fault loop probe and system	714/734